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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|---|
| **Applicant:** | Oliver Chyan, et al. | **Art Unit:** | 2818 |
| **Serial No.:** | 10/600,039 | **Examiner:** | Dung Ahn Lee |
| **Filed:** | 06/20/2003 | **Docket:** | 122302.00001 |

**Title:** **METHOD OF USING MATERIALS BASED ON RUTHENIUM AND IRIDIUM AND THEIR OXIDES, AS A CU DIFFUSION BARRIER, AND INTEGRATED CIRCUITS INCORPORATING THE SAME**

## 37 CFR 1.131 DECLARATION BY OLIVER CHYAN

May 11, 2005

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that the above correspondence is being mailed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 11, 2005.

Lisa Lynch

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir or Madam:

This Declaration is to establish completion of the invention of the above referenced United States Patent application (the "Application") in the United States at a date prior to February 5, 2002, which is the effective date of the prior art patent Omstead, United States Patent No. 6,713,373 B1 that was cited by the Examiner.

I, Oliver Chyan, having a home address of 2828 Southridge Drive, Denton, Texas, hereby declare that I am one of the named inventors of the above referenced patent application.

I further declare that prior to February 5, 2002, I did conceive and reduce to practice my invention including using Ruthenium ("Ru") and its oxides as a barrier layer on integrated circuits in place of more resistive tantalum/tantalum nitride barriers, as is evidenced by the attached documents.

Further, I exercised due diligence from the date of these documents until the filing of my patent application identified above. The first document dated April 1, 2001, comprise pages from my laboratory notebook describing the procedure of preparing Ru. This document recognizes the use of Ru and its oxides as a diffusion barrier for copper ("Cu") interconnects. The second document is a Project Summary page and accompanying Texas Advanced Technology Program Grant request dated October 2001 which recognizes that the invention can replace the more costly additional Cu-seed layer used in fabrication of integrated circuits as the invention facilitates direct Cu electrofill. The purpose of the grant was to further explore the invention of using a more conductive Ru based barrier stack (Ru, $RuO2$) to permit Cu electrofill without the Cu-seed layer.

These documents were archived in my notes, and the attached documents are a true copy of such documents.

This Declaration is made prior to final rejection.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully Submitted,

Oliver Chyan

Dr. Oliver Chyan

4/01/2001 Copper Electrochemical Deposition on Ruthenium

Purpose: To investigate the viability of Ru as a barrier layer IC circuits.

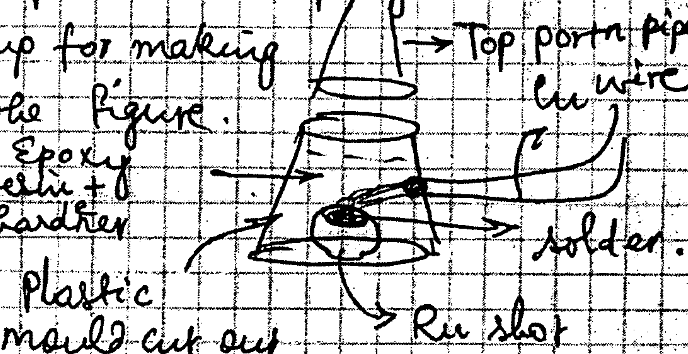
Procedure: 1. It was important to make a workable electrode out of ~~to~~ the odd shaped Ru shots.

2. Polishing of Ru wasn't easy, ∵ it is is 6.5 on Moh's mineral hardness scale. The following procedure was followed:-

(a) Made electrode out of the Leco epoxy and Resin.

(b) Used the kind of set-up for making the epoxy set as shown in the figure.

Takes at least 24 hrs to set hard.




(c) For polishing used 60, 180, ~~400~~ 320, 600 grit SiC abrasive; then 6μm & 1μm diam. suspension & then finally w/ 0.05μm γ-$Al_2O_3$ suspension for a mirror finish.

(d) Sonicated the electrode in between each grinding and polishing step.

(e) Subjected the Ru electrode to XRD to discern the phases existing in the procured Ru shot. Ru has a hcp structure. The peaks were of the expected relative intensities w/a consistent "blue-shift" by 0.4° from the normal values.

Model 270/250 Research Electrochemistry Software , v. 4.40
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Pstat: M273 [92,98] Ver 107
CA CHRONOAMPEROMETRY File Status: NORMAL
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Time Run: 11:30:57

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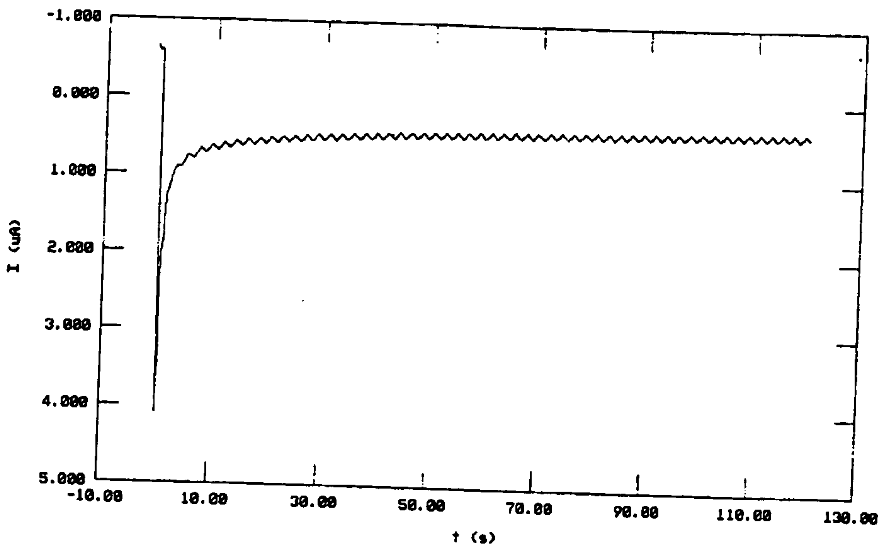
| E2 | PASS vs. R | ET | 5 S | T1 | 1.200E+02 | T2 | PASS |
| CR | AUTO | TP | 1.000E-01 | RU | 0.000E+00 | SO | Pass |
| IR | NONE | NP | 1200 | RT | HIGH STABILITY | | |
| REF | 0.22200 AgCl | FL | NONE | AR | 1.000E+00 | AU | NO |
| OC | 0.492 | WRK | SOLID | | | | |

—— ru8.dat

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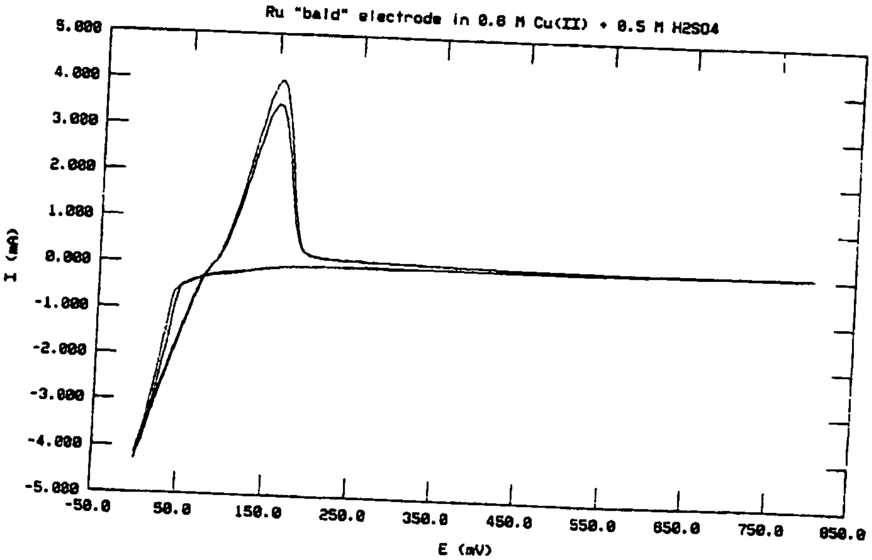
| V2 | 0.800 vs. R | FP | 0.800 vs. R | SI | 2.000E-03 | VD | PASS |
| SR | 1.000E-01 | ST | 2.000E-02 | NC | 2 | | |
| AM | 4/4 | CR | AUTO | NP | 1600 | SC | 1 |
| RU | 0.000E+00 | IR | NONE | FL | NONE | | |
| RT | HIGH STABILITY | REF | 0.22200 AgCl | WRK | SOLID | | |
| AR | 1.000E+00 | AU | NO | OC | 0.489 | | |

—— ru8.dat

Ru "bald" electrode in 0.8 M Cu(II) + 0.5 M H2SO4



Advanced Research Program/Advanced Technology Program – 2001

# Proposal Cover Page

| Proposal # (NOTE: This proposal # must be the same # as its preliminary Pre-proposal) | Targeted Research Area (must be the same research area as its preliminary Pre-proposal) | Program ("X" one) ARP ☐ ATP ☒ TDT ☐ |
|---|---|---|
| 003594-0078-2001 | Materials Technology | |

**Name and Address of Submitting Organization to which award should be made (include branch/campus/other components)**

Office of Research Services
P.O. Box 305250
University of North Texas
Denton, TX 76203

Is this a collaborative proposal with another institution? No X Yes ___
If yes, please complete this block and Page Proposal – 1A.
Name(s) of collaborating institution(s) and amounts requested for each institution. (NOTE: Collaborating institution(s) must be eligible institution(s) as defined under program guidelines.)

| Institution | Requested Amount |
|---|---|
| | |

**Title of Proposed Project (maximum of 100 characters)**

Developing a New Ruthenium-based Diffusion Barrier for Copper Interconnects

**Total Amount Requested for Project**

$264,890

**Keyword Descriptors of Research (maximum of 5 keywords, maximum of 25 characters per keyword)**

Ruthenium, Copper Interconnects, Cu Plating, Diffusion Barrier, and Cu Diffusion

**Technology Development & Transfer proposals only:**

Is this proposal based on a previous ARP or ATP Project? No X Yes ____ If yes, list project number for the previous ARP or ATP project and year it was funded: ARP____________ ATP____________ 1987 1989 1991 1993 1995 1997 1999

Is this work based on other previously sponsored research? If yes, list sponsor, project title, and funding period.

| Sponsor | Title | Funding Period |
|---|---|---|
| | | |

Name(s) of matching company and dollar amount committed (total industry support amount must be equal to or greater than the requested amount)

Texas companies:

| Company | Amount | Company | Amount |
|---|---|---|---|
| | | | |

Other companies:

| Company | Amount | Company | Amount |
|---|---|---|---|
| | | | |


**Principal Investigator's Name (type or print)**

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Principal Investigator's ARP/ATP On-line System User Number

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Signature

**Authorized Institutional Representative's Name, Title, Phone Number, FAX Number, E-Mail Address (type or print)**

Reata Busby, Director, Office of Research Services
940-565-3940
940-565-4277 (fax)
Rbusby@unt.edu


I certify that this institution has a written Organizational Accountability System in place as described in Grant Condition #1.

Reata Busby 8/13/01

Signature Date

# Project Summary

| Proposal # 003594-0078-2001 | Principal Investigator(s) Oliver Chyan | Institution University of North Texas |
|---|---|---|
| Program ("X" one) ARP ☐ ATP ☒ TDT ☐<br>Research Area Material Technology | | PI's Mailing Address (including department), Phone Number and Internet Address<br>University of North Texas<br>Department of Chemistry<br>P.O. Box 305070<br>Denton, TX 76203<br>940-565-3463; chyan@unt.edu |
| Title of Proposal<br>Developing a New Ruthenium-based Diffusion Barrier for Copper Interconnects | | |

NOTE: This abstract should be suitable for public release. (Double-spaced, 11-point minimum font size.)

The overall objective of this proposal is to explore a new and promising ruthenium-based copper diffusion barrier material that will replace the more resistive tantalum/tantalum nitride barrier and eliminate a costly additional Cu-seed layer currently used in the fabrication of integrated circuits. Microprocessing chips fabricated with more conductive copper (Cu) interconnects and low-k dielectrics will operate with less power and at significantly higher speed. However, a rather complex stack structure of tantalum nitide/tantalum/Cu-seed is required in the damascene trench/via features to prevent catastrophic contamination caused by Cu diffusion. Our proposed study will utilize a more conductive ruthenium-based barrier stack (Ru, $RuO_2$) to afford direct Cu electrofill without the additional Cu-seed layer. Our preliminary data show that Cu plates easily and exhibits excellent adhesion on ruthenium substrates. More importantly, X-ray diffraction patterns demonstrate an excellent chemical stability of Cu/Ru interface, vital for an effective Cu diffusion barrier, even after annealing at 800 °C. A substantial leveraging of the funds requested is made possible by a local microelectronic company and UNT. We anticipate that the elimination of the Cu-seed layer will decrease copper interconnect processing costs, which now account for 50% of the wafer processing expenditures, further simplifying circuit design and promoting overall integration success. The proposed study, at its completion, is expected to significantly benefit the Texas microelectronic industry.

*Research Objectives*

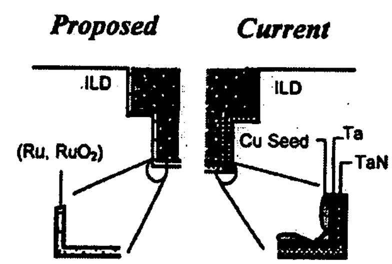
The key thrust of this advanced technology proposal is to explore a new and promising ruthenium-based diffusion barrier material that will replace a more resistive Ta/TaN barrier and eliminate the need for an additional Cu-seed layer. The elimination of the Cu-seed layer will decrease interconnect processing costs, which now account for 50% of the wafer processing expenditures, and further simplify circuit design and promote overall integration success.

In the sub-0.13 μm generation of integrated circuits (IC), copper (Cu) will completely replace aluminum as the new interconnect material due to its favorable electrical conductivity (1.67 $\mu\Omega$.cm vs. 2.66 $\mu\Omega$.cm of aluminum) and its superior resistance to electromigration.[1] Improved electromigration resistance allows integrated circuits to operate at higher current densities and possibly at higher temperatures. IC chips fabricated with more conductive Cu interconnects and low-k dielectrics operate with less power and at significantly higher speed due to decreases in the interconnect RC coupling delay. The new dual-damascene patterning process[2] coupling with chemical-mechanical planarization[3,4] (CMP) significantly simplifies Cu interconnect routing and lowers manufacturing costs.

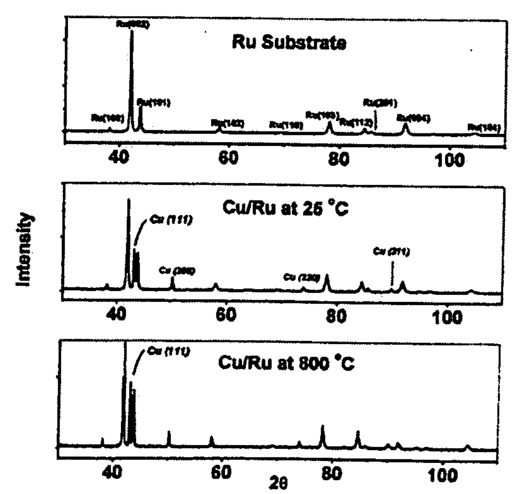
However, copper diffuses easily into active silicon devices and interlayer dielectrics (ILD), especially under electrical and thermal stresses.[5] To prevent catastrophic contamination caused by Cu diffusion, diffusion barriers like tantalum (Ta) and tantalum nitride (TaN) are currently used in the damascene trench/via features to contain Cu interconnects.[6,7] Ideal diffusion barriers should have good adhesion to both copper and interlayer dielectrics, in addition to affording a conductive Cu plating platform that allows for the bottom-up Cu electrofill of damascene features. Since thin barrier layers of Ta (13.2$\mu\Omega$.cm) and TaN (>200$\mu\Omega$.cm) are too resistive to plate Cu directly, a continuous Cu-seeding layer (>7.5nm) must be deposited over the Ta/TaN barrier to assure a good Cu electrofill.

The most challenging aspect of implementing Cu interconnects for near-term (<5 years) CMOS applications beyond the 100 nm mode is the increasing difficulty with the overall

process integration.[8] Shrinking dimensions demand an increasingly high-aspect-ratio of trench/via features that make PVD barrier/seed deposition and Cu electrofill more difficult. Any discontinuities in the Cu seed layer, large overhang, or poor coverage on the lower sidewall can affect the Cu electroplating through an early pinch-off of the structure, resulting in a void defect being formed. Structural integrity concerns and adhesion issues of the barrier metal to the new ultra low-k dielectric are often mentioned as accompanying problems.




Our proposed study will focus on utilizing a more conductive barrier, Ru/$RuO_2$, to replace Ta/TaN and afford direct Cu electrofill without the need of an additional Cu seed layer. Ru is an air-stable transition metal of high melting point (2310 °C) that has nearly twice the electrical conductivity (7.6$\mu\Omega$.cm) and thermal conductivity as Ta (Appendix, Figure 1), Furthermore, Ru, like Ta, shows negligible solid solubility with Cu at 900 °C based on the binary phase diagram (Figure 1). Our preliminary data show that Cu plates easily (Appendix, Figure 2) and exhibits excellent adhesion (by Scotch tape peel test) on Ru substrates. More importantly, X-ray diffraction (XRD) patterns (see right), indicated **no** new phases or intermetallic compound formation between the Cu deposit and Ru substrate *even after annealing at 800 °C.* The observed chemical stability of the Cu/Ru interface under high thermal stress underscores the potential of Ru as an effective Cu diffusion barrier. The XRD data also reveal favorable heteroepitaxial growth of Cu by electroplating on Ru with strong Cu(111) texture. Enhanced Cu(111) texture has been shown to reduce defects at the interface and improve the electromigration reliability of Cu interconnects.[9]



Metal inter-diffusion will occur if mixing leads to a lowering of the free energy of interface. Gjostein[10] studied various diffusion mechanisms in fcc metals (like Cu) and showed diffusion in thin non-epitaxial films is dominated by grain boundaries and dislocations. In contrast to the resistive TaN barrier, $RuO_2$ has a metal-like conductivity (35 $\mu\Omega$.cm) resulting from a partial filling of the Ru-O $\pi^*$ band in its tetragonal rutile structure.[11] It is worthy of noting that conductive $RuO_2$ has been used as the barrier layer for aluminum interconnects.[12] Increased use of the Ru/$RuO_2$ stack as the contact electrode in new PZT ferroelectric devices has also been reported.[13-15] Our proposed study will utilize the stack structure of Ru/$RuO_2$ to prevent the grain boundary diffusion of Cu into the Ru barrier layer. Previously, Nicolet and others[16] have shown that "stuffing" the grain boundaries and dislocations with impurities like oxygen and nitrogen effectively retards Cu diffusion through such paths. We anticipate that a relatively thin layer of $RuO_2$ on Ru will suffice as a barrier function and still allow direct Cu plating without the Cu-seed layer. However, Cu may not effectively wet $RuO_2$ surfaces. A thin coating of Ru over the Ru/$RuO_2$ stack (equivalent to Ru/$RuO_2$/Ru stack) by electroplating or sputtering may be necessary to ensure Cu wetting.

***Methodology***

We will study the electrodeposition of Cu on Ru and Ru/$RuO_2$ substrates to establish the plating characteristics and adhesion (i.e. Cu wetting) properties vital to the bottom-up Cu electrofill process. The Chyan lab has shown that electrochemically deposited Cu on Ru exhibits excellent adhesion properties. $RuO_2$ will be grown electrochemically or by thermal oxidation of the Ru metal substrate. Metallurgical interactions between Cu/Ru and Cu/$RuO_2$/Ru under thermal stress will be examined by XRD, XPS depth profiling, RBS and adhesion tests. Nucleation and growth of Cu plating will be engineered toward larger Cu grain for better electromigration reliability and conductivity of Cu interconnects (Appendix, Figure 3).

The technology basis of fabricating Ru, $RuO_2$ and Ru/$RuO_2$ for our proposed study is readily available from the published literature.[13-15,17] Ru and $RuO_2$ can be deposited by reactive ion sputtering, chemical vapor deposition or electrochemical deposition. Electroless plating to provide conformal step coverage of Ru on ILD coated silicon substrate will be attempted. We will explore the feasibility of fabricating Cu/Ru/$RuO_2$, Cu/$RuO_2$/Ru, or Cu/Ru/$RuO_2$/Ru on ILDs by an all-electrochemical process. If successful, the interconnect fabrication process will be significantly streamlined.

To accomplish the inter-diffusion study, we will utilize the facilities in the new Laboratory for Electronic Materials and Devices (*vide infra*) at UNT to fabricate a stack structure of Cu/(Ru, $RuO_2$) on an oxide coated silicon test wafer. The exact configuration of the (Ru, $RuO_2$) barrier layer will be determined by how Cu wets $RuO_2$. After annealing under a $N_2$ atmosphere up to 800 °C, the extent of metallic inter-diffusion will be characterized by XPS, Auger electron spectroscopy via $Ar^+$ ion depth profiling and RBS. For the best interfacial sensitivity, TOF-SIMS depth profiling analysis (service provided by Texas Instruments) using 12 KeV $Ga^+$ ion sputtering gun at low incident angle will be used. The TOF-SIMS detected area will be kept within a small fraction of sputtered area to avoid crater sidewall contribution and improve depth resolution. The diffusion depth with respect to each annealing temperature will be determined. The diffusion coefficient constant assimilated from experimental results will be compared with data reported[18] for the Cu/Ta and Cu/TaN/Ta systems. Cross sectional SEM /TEM and resistivity probe data will provide morphological and electrical properties of the Cu/(Ru, $RuO_2$) stack throughout the annealing process.

For the sub-0.13 μm generation IC chips, adhesion between barrier layer and new low-k ILDs will be a critical issue on manufacturability. Through the careful selection of suitable ruthenium precursors (Appendix, Figure 4) we can control the extent of Ru coverage and engineer strong interfacial chemical bonding that is required for enhanced adhesion between the Ru, $RuO_2$ and new low-k materials. This will lead to superior mechanical strength, critical

to the CMP process. Several of the chosen compounds[19] in Figure 4 are expected to afford Ru films under milder conditions than the Ru compounds utilized to date[20] because of the labile ancillary ligands present. The prospect of controlling the film concentration of Ru via the nuclearity of the different clusters will be explored, and the use of the nitrido-based clusters $HRu_5N(CO)_{14}$ and $HRu_6N(CO)_{16}$ to directly stuff the grain boundaries through the incorporation of nitrogen atoms *in situ* will be investigated.

*Proposed Timeline*: We anticipate that the first 6-8 months will be devoted to the Cu electroplating on Ru and $Ru/RuO_2$, adhesion/Cu wetting, testing Ru MOCVD precursors and thermal annealing studies. Based on the Cu-wetting results obtained, the second 6-8 months will be devoted to design and Cu/(Ru, $RuO_2$) stack fabrication on ILD coated wafers supplied by TI, followed by inter-diffusion/annealing studies to probe the barrier effectiveness. In depth interfacial characterization (diffusion properties, chemical binding, adhesion, morphology etc.) will be carried out using XPS, TOP-SIMS, AFM and RBS throughout the research program.

*Research Personnel*

Oliver Chyan/PI has more than fifteen years of research experience on silicon surface characterization, semiconductor materials chemistry, and electrochemistry. He has a Ph.D. in Chemistry from MIT (M. Wrighton). Dr. Chyan will supervise two graduate students and two undergrads in exploring the new ruthenium-based Cu diffusion barrier work. The undergrad assistants will be recruited from the Texas Academy of Mathematics and Sciences at UNT.

Michael Richmond/co-PI has extensive experience in organometallic chemistry and has published over 120 papers, much of which focused on transition-metal chemistry. He has a Ph.D. in Chemistry from the University of Alabama (C. Pittman). Dr. Richmond will supervise the MOCVD and adhesion improvement of Ru and $RuO_2$ on interlayer dielectrics with a graduate and an undergraduate student.

### *Technology Transfer*

The major technology transfer mode envisioned will be through Texas Instruments and other Texas-based IC industries. The Chyan research group has an established and on-going collaborative relationship with both Texas Instruments and SEMATECH. These collaborative interactions include teleconferences, presentations at meetings, conferences, national symposia, as well as publications and patent applications (if appropriate). We expect the technology transfer from UNT to industry will be effective since the in-place collaborative infrastructures have already allowed research personnel from UNT and industry to work closely together.

### *Institutional Commitment and Additional Sources of Support*

Exceptionally well-equipped laboratories and office space are available at UNT for this work. We will utilize facilities in the new **Laboratory for Electronic Materials and Devices (LEMD, www.mtsc.unt.edu/lemd)** for the proposed ruthenium-based diffusion barrier work. The LEMD lab includes an extensive ultrahigh vacuum research clustertool permits a combination of molecular beam epitaxy (MBE), physical vapor deposition (PVD) and Chemical Vapor Deposition (CVD) techniques with film physical (RBS, XPS, UPS, AES, STM) and electrical (CV, IV) characterization. Ru thin films can be sputter-deposited using a RF/DC sputter (Torrus) on an oxide coated silicon wafer which can be transported between the chambers in an evacuated tube to preserve surface/film integrity. A comprehensive surface analysis system is also housed in the LEMD and provides X-ray Photoelectron Spectroscopy (standard Al/Mg and monochromatic Al sources), Ultraviolet Photoelectron Spectroscopy (He, Ne sources), Auger Electron Spectroscopy and Ar ion depth profiling capabilities. Rutherford Backscattering Spectrometry (RBS) on Cu/(Ru, $RuO_2$)/IDLs/Silicon samples will be performed in the LEMD with a NEC 9-SH Pelletron Van de Graff accelerator. The labs of both PI's are